M.2 Updates

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Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

Agenda

- **Review changes to the M.2 Specification Post Rev 1.1**
- **Review errata for Rev 1.1**
- **Review 8GT/s compliance proposal for M.2**
- **Review 16GT/s compliance proposal for M.2**
- **Timeline**

Approved ECNs post Rev 1.1

- **ECNs Approved post Rev 1.1 Specification Release:**
  - PCIe® BGA SSD 11.5x13
  - Enable PCIe and USB 3.1 Gen-1 on M.2 Card Key B
  - Add a second PCIe lane to Type 1216 SDIO based LGA Module
  - Additional voltage value for PWR_1 rail
  - NCTF Ground ball definition for PCIe BGA SSD 11.5x13

PCIe BGA SSD 11.5x13 Key Deltas vs. the 16x20 BGA

- **<1/2 the size: 150mm² vs. 320mm²**
  - Better fit in small form factor applications
- **Only supports x2 PCIe**
  - no x4 or SATA support
- **Inner balls are NC**
  - Allows for dual footprint of storage device with other mobile storage devices (eMMC and UFS)[1]
- **Optional SPI interface**
  - For optional NOR support

1. eMMC and UFS specs are managed by JEDEC

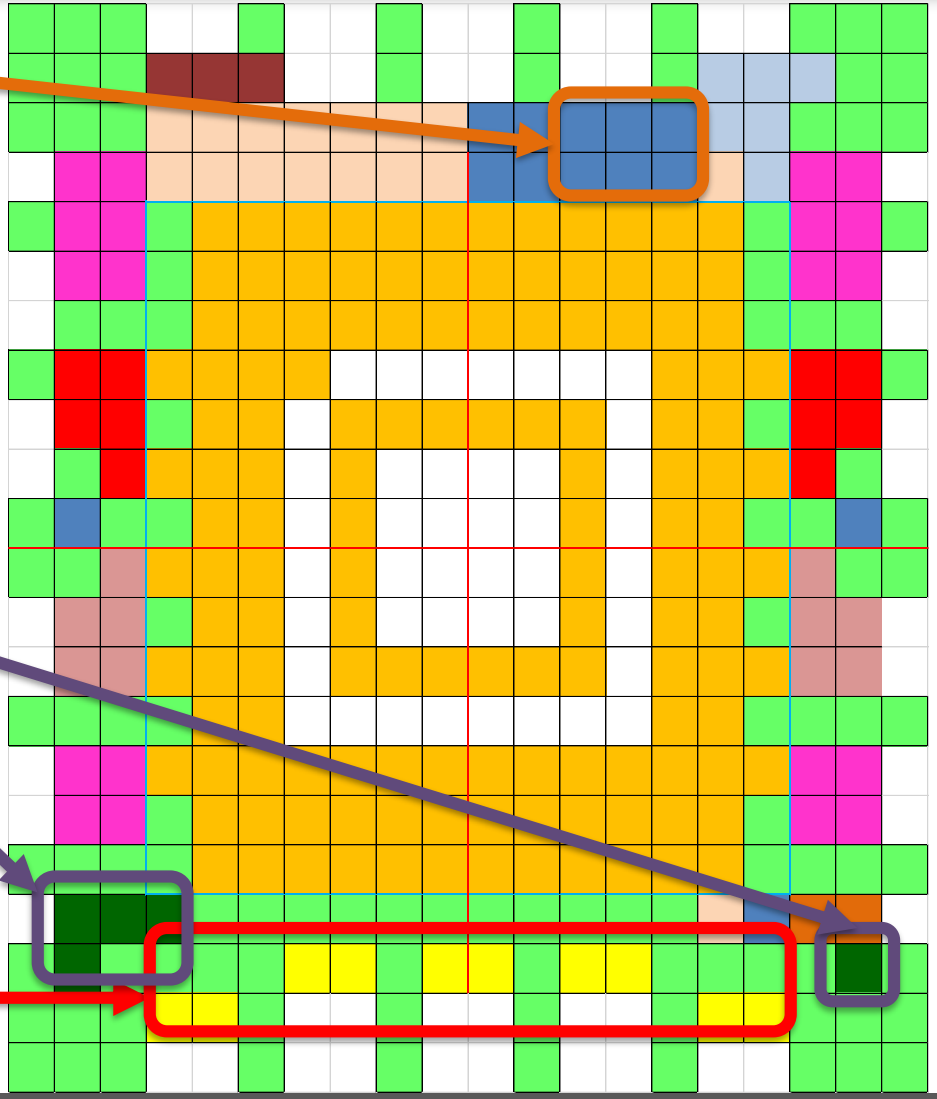
Other Changes

- **Multiple Voltage range support**
  - 16x20 spec introduced 3 voltages: 3.3 V, 1.8 V, and 1.2 V
  - 11.5x13 spec keeps 3 supplies but makes the power rail support device specific for flexibility.
    - Future ECN's could introduce additional voltages.

Pin Name (Nominal Voltage)	Voltage Range	Platform Rail Type
PWR_1 (+3.3 V)	2.8 V to 3.6 V	Always On
PWR_2 (+1.8 V)	1.7 V to 1.9 V	Always On
PWR_2 (+1.2 V) PWR_3 (+1.2 V)	1.14 V to 1.26 V	Always On
PWR_3 (+1.1 V)	1.06 V to 1.17 V	Always On
PWR_3 (+0.9 V)	0.86 V to 0.98 V	Always On

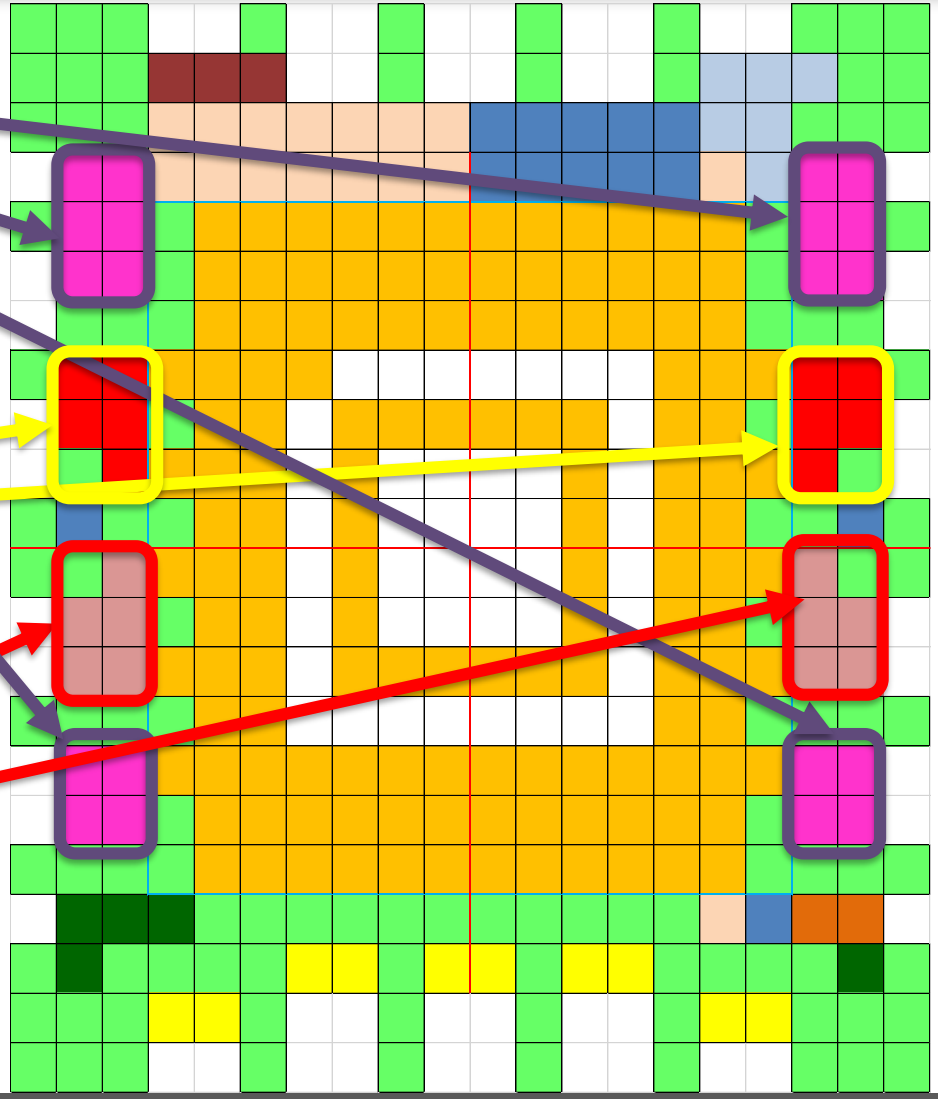
Ballout Details -1

- **JTAG signals**
- **PCIe sideband**
- **PCIe lanes (x2)**



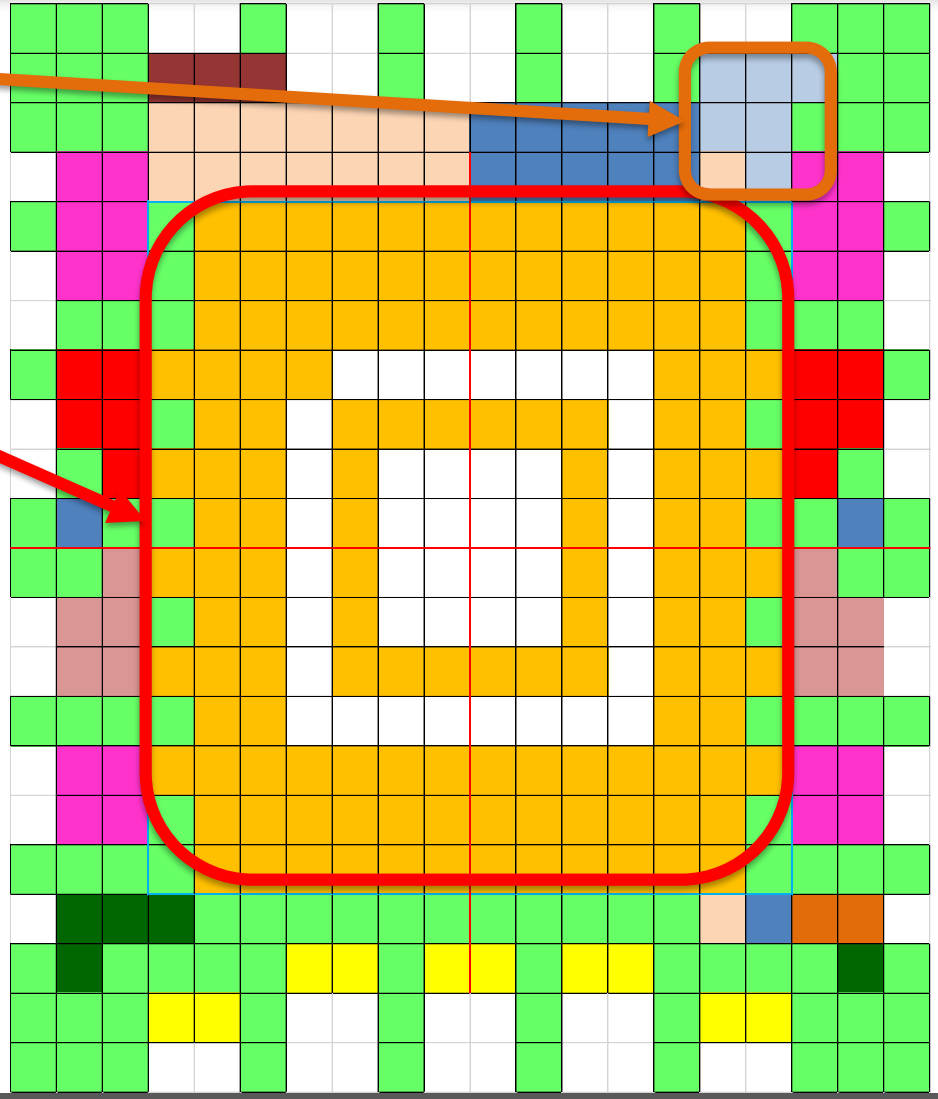
Ballout Details -2

- **PWR_2**
- **PWR_1**
- **PWR_3**



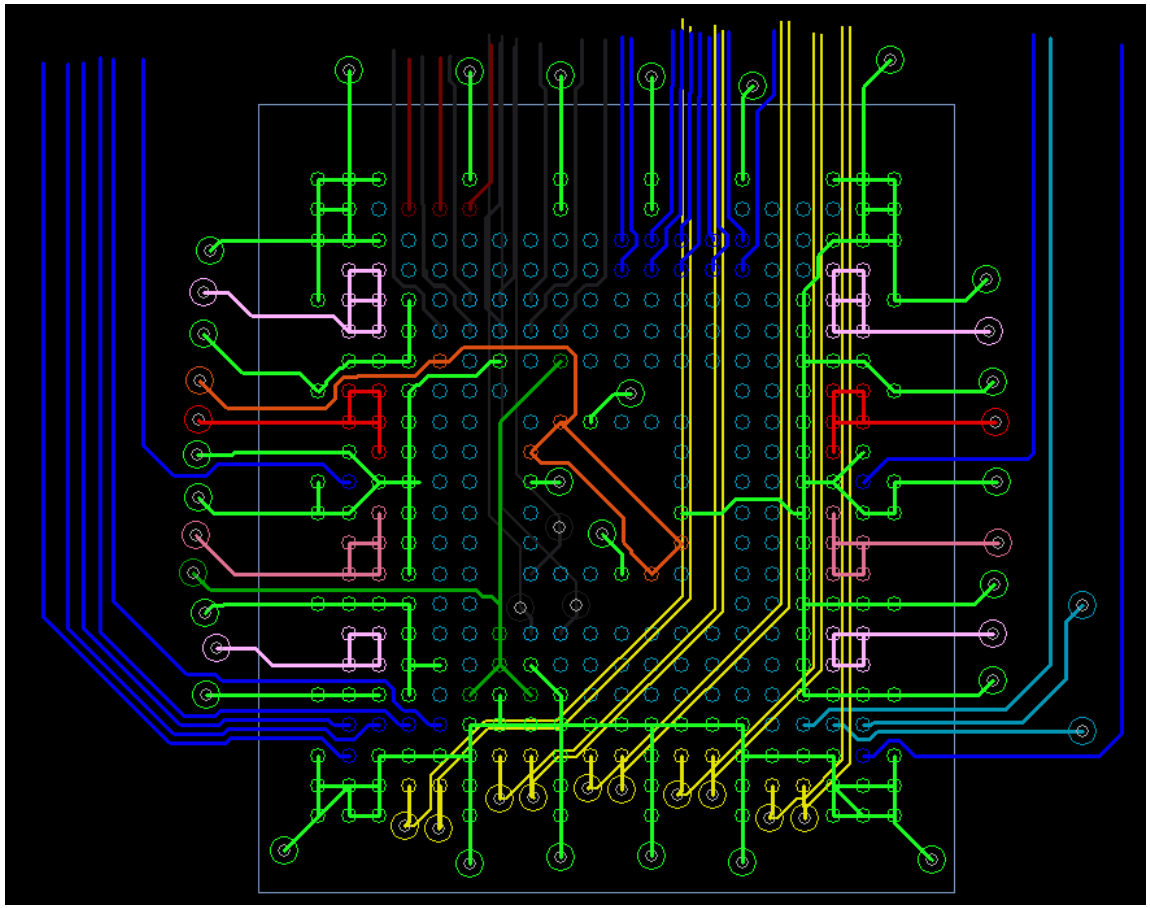
Ballout Details -3

- **SPI Port (Optional)**
- **NC pins (along with a few grounds)**
  - This area can support other storage interfaces



Routing Study

- **The ballout is friendly to Type 3 or Type 4 PCBs**



Enable PCIe and USB 3.1 Gen-1 on M.2 Card Key B ECN

- **WWAN Key-B modified to enable PCIe and USB 3.1 Gen1 signals simultaneously**
- **Configuration States 4, 5, 6 and 7 modified**
- **Configuration State 14 re-defined**
- **Pinout tables updated to reflect the changes**

Enable PCIe and USB 3.1 Gen-1 on M.2 Card Key B ECN

State #	Add-in Card Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – PCIe, USB3.1 Gen1	0[4, 5]
5	GND	NC	GND	NC	WWAN – PCIe, USB3.1 Gen1	1[4, 5]
6	GND	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	2[4, 5]
7	GND	NC	NC	NC	WWAN – PCIe, USB3.1 Gen1	3[4, 5]
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
~~14~~	~~NC~~	~~GND~~	~~NC~~	~~NC~~	~~RFU~~	~~N/A~~
14	N/C	GND	N/C	N/C	WWAN – PCIe, USB3.1 Gen1	Vendor Defined[3, 5]
15	NC	NC	NC	NC	No Add-in Card Present	N/A

Enable PCIe and USB 3.1 Gen-1 on M.2 Card Key B ECN

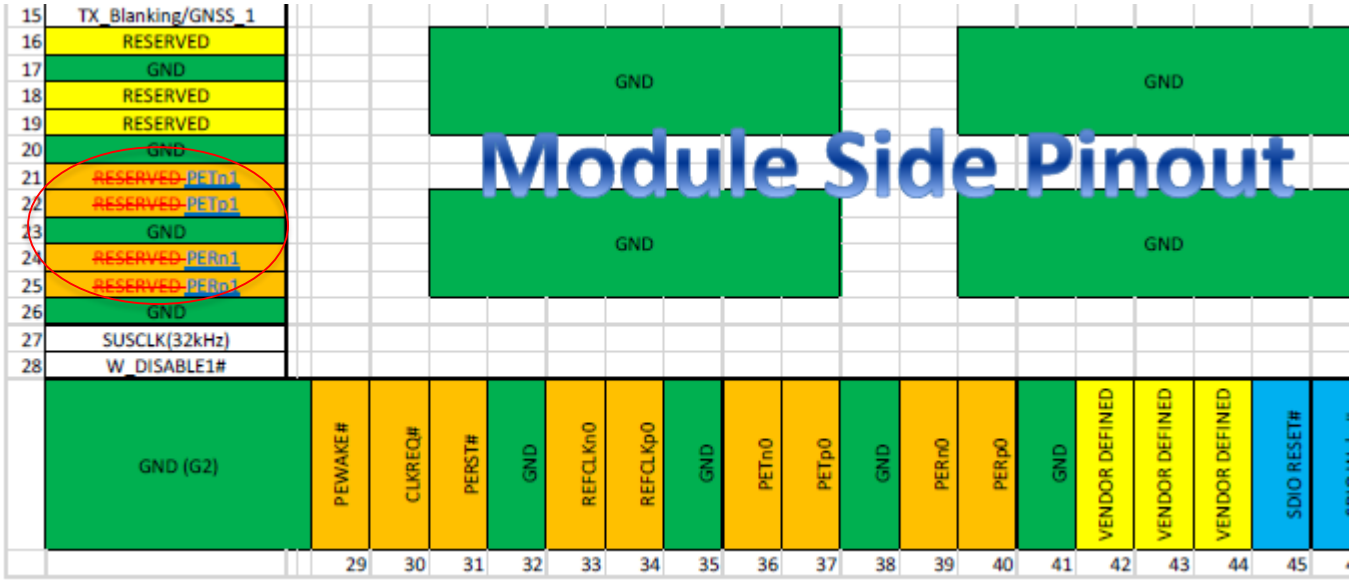
Table 32x. Socket 2 Key B PCIe/USB3.1 Gen1-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
74	3.3V	CONFIG_2 (States 4, 5, 6, 7 and 14)	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 4, 5, 6, 7 and 14)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	N/C	ANTCTL0 (O)(0/1.8V)	59
56	N/C	GND	57
54	PEWAKE# (I/O)(0/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/3.3V)	REFCLKn	53
50	PERST# (I)(0/3.3V)	GND	51
48	VENDOR DEFINED or GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERp0	49
46	VENDOR DEFINED or GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	PERn0	47
44	VENDOR DEFINED or GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	GND	45
42	VENDOR DEFINED or GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETp0	43
40	VENDOR DEFINED or GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	PETn0	41
38	N/C	GND	39
36	UIM-PWR (O)	USB3.1-Rx+	37
34	UIM-DATA (I/O)	USB3.1-Rx-	35
32	UIM-CLK (O)	GND	33
30	UIM-RESET (O)	USB3.1-Tx+	31
28	VENDOR DEFINED or GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	USB3.1-Tx-	29
26	VENDOR DEFINED or GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2#	GND	27

Add a Second PCIe Lane to Type 1216 SDIO Based LGA Module

- **Type 1216 Connectivity Module pinout modified to add second PCIe lane**
- **Pins reserved previously**
- **Connectivity modules needing higher bandwidth can be implemented as LGA in addition to Add-in Card**

Add a Second PCIe Lane to Type 1216 SDIO Based LGA Module



Additional Voltage Value for PWR_1 Rail

- **Additional voltage value added to the PWR_1 rail in the PCIe BGA SSD 11.5x13 ECN**
- **PWR_1 rail supports 2.5 V in addition to 3.3 V**
- **Supports trend to accommodate lower NAND array power supply voltage**
- **Simple design- no power regulators**

Additional Voltage Value for PWR_1 Rail

3.4 BGA SSD Interface Signals

Table 39 BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, 2828

Category	Signal Name	I/O	Function	IO Voltage
Power and Grounds	PWR_1[1] (8 pins)	I	+3.3 V or +2.5V source	
	PWR_2[1] (12 pins)	I	+1.8 V or +1.2 V[1] source	

Nominal Voltage	Voltage Range	Platform Rail Type
+3.3 V	2.8 V to 3.6 V	Always On
+2.5V	2.45 V to 2.75 V	Always On
+1.8 V	1.7 V to 1.9 V	Always On
+1.2 V	1.14 V to 1.26 V	Always On
+1.1 V	1.06 V to 1.17 V	Always On
+0.9 V	0.86 V to 0.98 V	Always On

NCTF Ground Ball Definition for PCIe BGA SSD 11.5x13

- **Redefines the outer most ring of ground pins in the 11.5x13 BGA SSD ball map to be redundant ground pins that are non-critical to function (NCTF).**
- **Pins connected to Host and Device GND but they are not critical pins**
- **Allow mechanical failures but not functional failure**

NCTF Ground Ball Definition for PCIe BGA SSD 11.5x13

3.4.4.7. NCTF (Non Critical To Function)

Signals documented as NCTF are redundant ground balls. They are connected to host ground and redundant to other device grounds, so the loss of the solder joint continuity due to mechanical failure at end of life conditions will not affect the overall product functionality.

Review Errata for Rev 1.1

- **Formatting issue in pages 183-186 of the M.2 Specification Rev 1.1**
- **Errata to be released soon**

Review Updates Post Rev 1.1

- **Figures added to support S4 and S5 Heights**

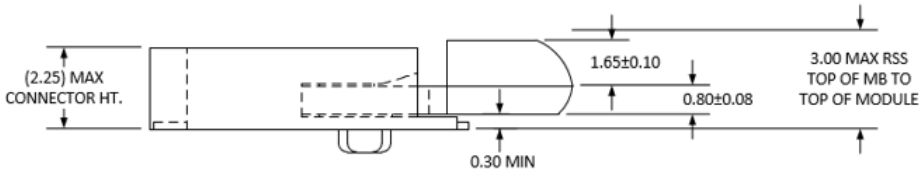


Figure: H2.3-S4- Stack-up Top Mount Single-sided Add-in Card for 1.75 Maximum Top-side Component Height and with Higher Clearance above Motherboard

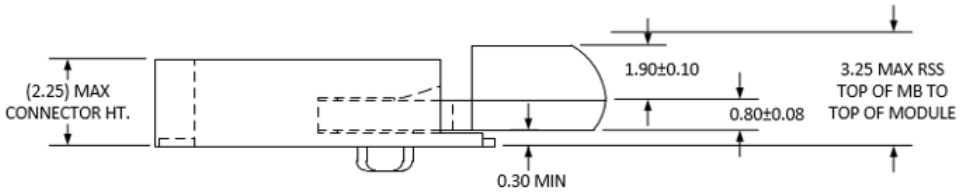


Figure: H2.3-S5- Stack-up Top Mount Single-sided Add-in Card for 2.00 Maximum Top-side Component Height and with Higher Clearance above Motherboard

Review Updates Post Rev 1.1

- **Figures added to support S4 and S5 Heights**

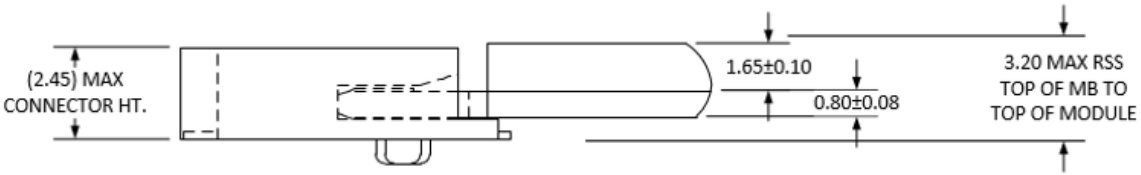


Figure: H2.5-S4- Stack-up Top Mount Single-sided Add-in Card for 1.75 Maximum Top-side Component Height and with Higher Clearance above Motherboard

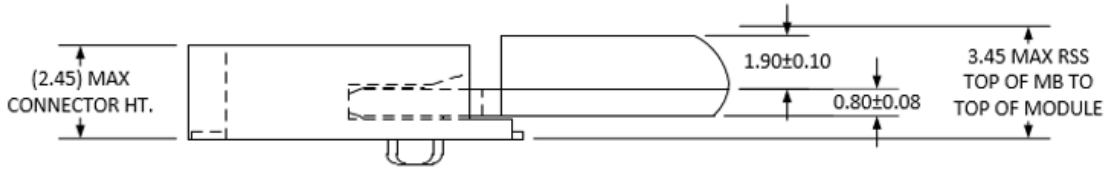


Figure: H2.5-S5- Stack-up Top Mount Single-sided Add-in Card for 2.00 Maximum Top-side Component Height and with Higher Clearance above Motherboard

Review Updates Post Rev 1.1

- **V_{BAT} related clarification:**
  - Clarify that V_{BAT} is applicable to WWAN-specific M.2 Adapters only. It does not apply to other Socket-2 Adapters such as SSDs.
  - Pinout for Socket-2 Key-B and Key-C corrected to indicate power pins as 3.3V/V_{BAT} instead of 3.3V.
  - Add clarification that FULL_CARD_POWER_OFF# is intended for WWAN-specific socket-2 Adapters working off V_{BAT}.

Review 8GT/s Compliance Proposal for M.2 SSDs

(Work in progress - subject to change)

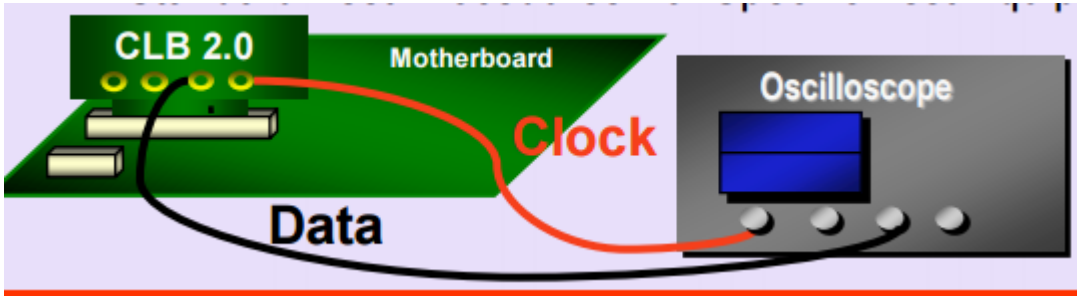
8GT/s Compliance Proposal for M.2

- **SEG considering to develop compliance program for M.2 SSDs supporting 8GT/s (and 16GT/s in future)**
- **Only Socket-3, Key-M supported**
  - Other sockets and keys not supported
- **Still under development**
  - Compliance program details being worked out in the SEG

Host TX Test Using CLB

- M.2 CLB 3.0 Standard Test Fixture connected to slot under test
- Lane under test and clock connected through CLB to oscilloscope
- Motherboard under test enters compliance mode
- CLB is TX and RX break out only
  - CLB does not provide features to select different compliance speeds and de-emphasis levels
  - An external pulse generator or CEM 3.0/4.0 CBB can be used to generate the compliance toggle pulse
- Data lane and reference clock sampled simultaneously
- 25 ps or smaller sample interval. At least 1 million UI.
- Standard Post Processing Analysis Software (Sigtest- to be updated to support M.2 templates)
  - Supports All Common RT Scope Data Formats
- Standard Test Procedures to be developed for specific test equipment

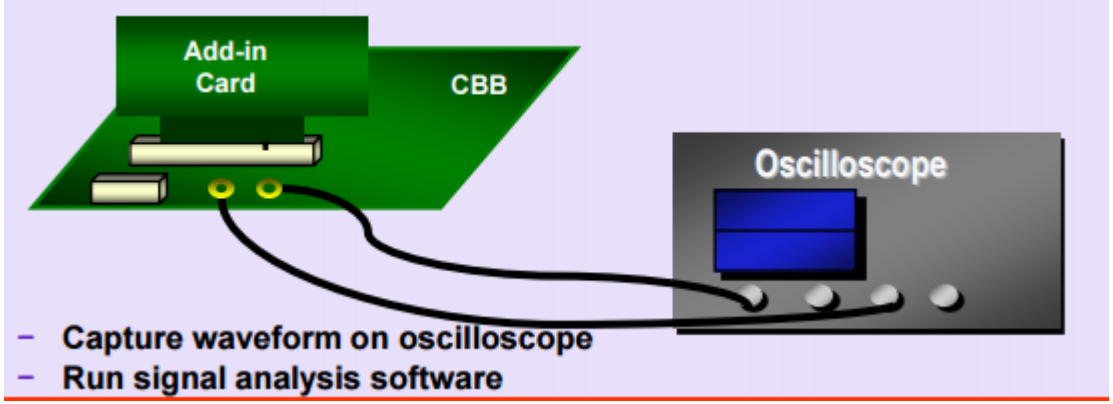
Host TX Test Using CLB



Add-in Card TX Test Using CBB

- Add-in Card under test plugged into M.2 CBB 3.0 Standard Test Fixture
- Lane under test connected through fixture to oscilloscope
- Add-in Card under test enters compliance mode
- Fixture provides features to select different compliance speeds and de-emphasis levels
- Data lane sampled
- 25 ps or smaller sample interval. At least 1 million UI.
- Standard Post Processing Analysis Software (Sigtest)
  - Supports all common RT Scope data formats
- Standard Test Procedures to be developed for specific test equipment

Add-in Card TX Test Using CBB



M.2 Test Fixture Outline

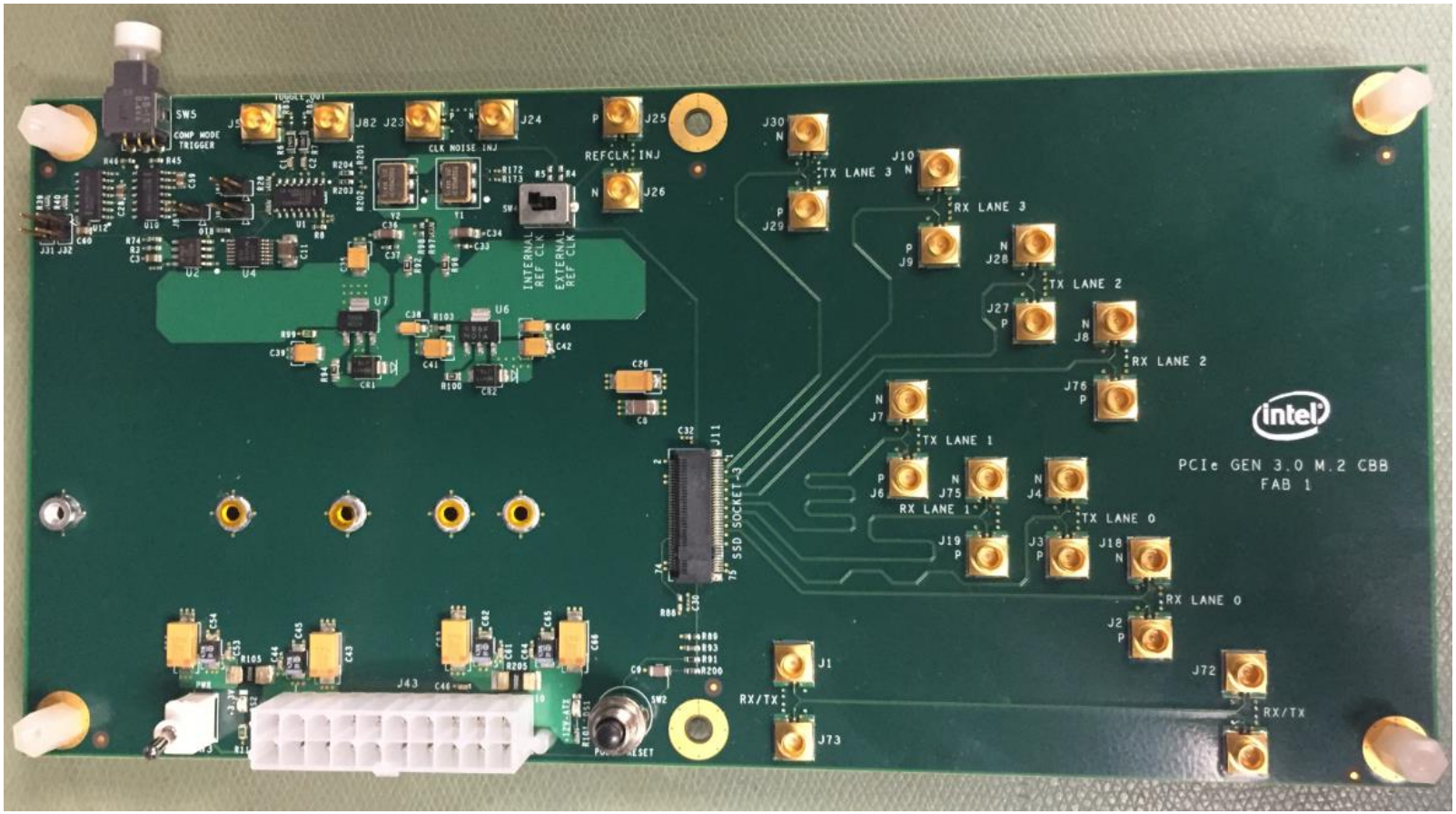
- **Test fixture supports Socket 3 M-key**
- **M.2 test fixture will include CLB and CBB, and employ similar testing methods to CEM 3.0**
- **Sizes 2230, 2280, and 22110 will be supported**

Fixture Development

- **Due to spatial constraints, multiple compliance load boards (CLB) per size are necessary to support all 4 data lanes.**
  - **Size 2230**
    - 4 CLBs
    - Each CLB supports 1 lane
  - **Size 2280**
    - 2 CLBs
    - Each CLB supports 2 lanes
  - **Size 22110**
    - 2 CLBs
    - Each CLB supports 2 lanes

M.2 CLB Prototypes

M.2 CBB Prototype



Review 8GT/s Compliance Proposal for M.2

- **Fixture Break Out Lengths**

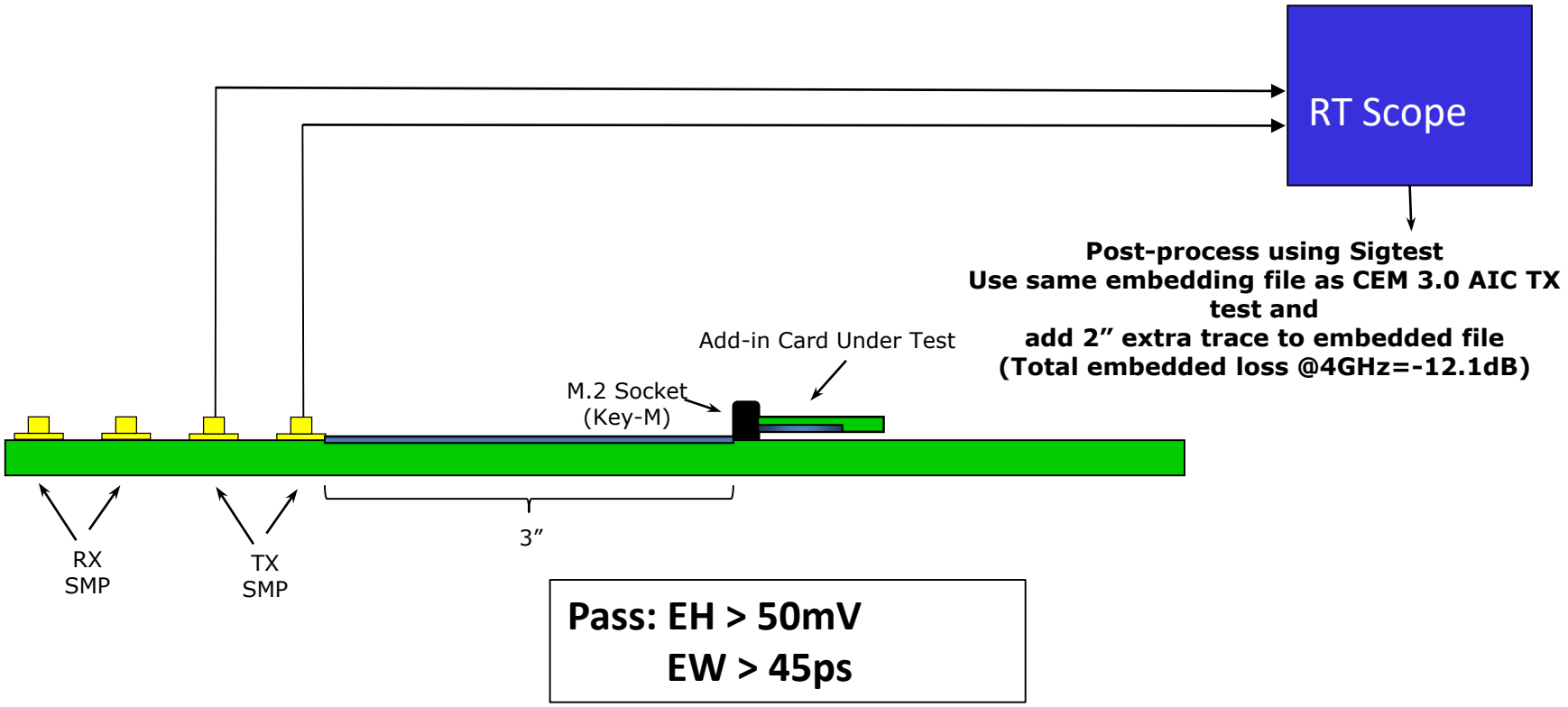
CLB	TX	RX
2230	2”	2”
2280	2”	2”
22110	2”	2”

CBB	TX	RX
	3”	3”

Assumptions

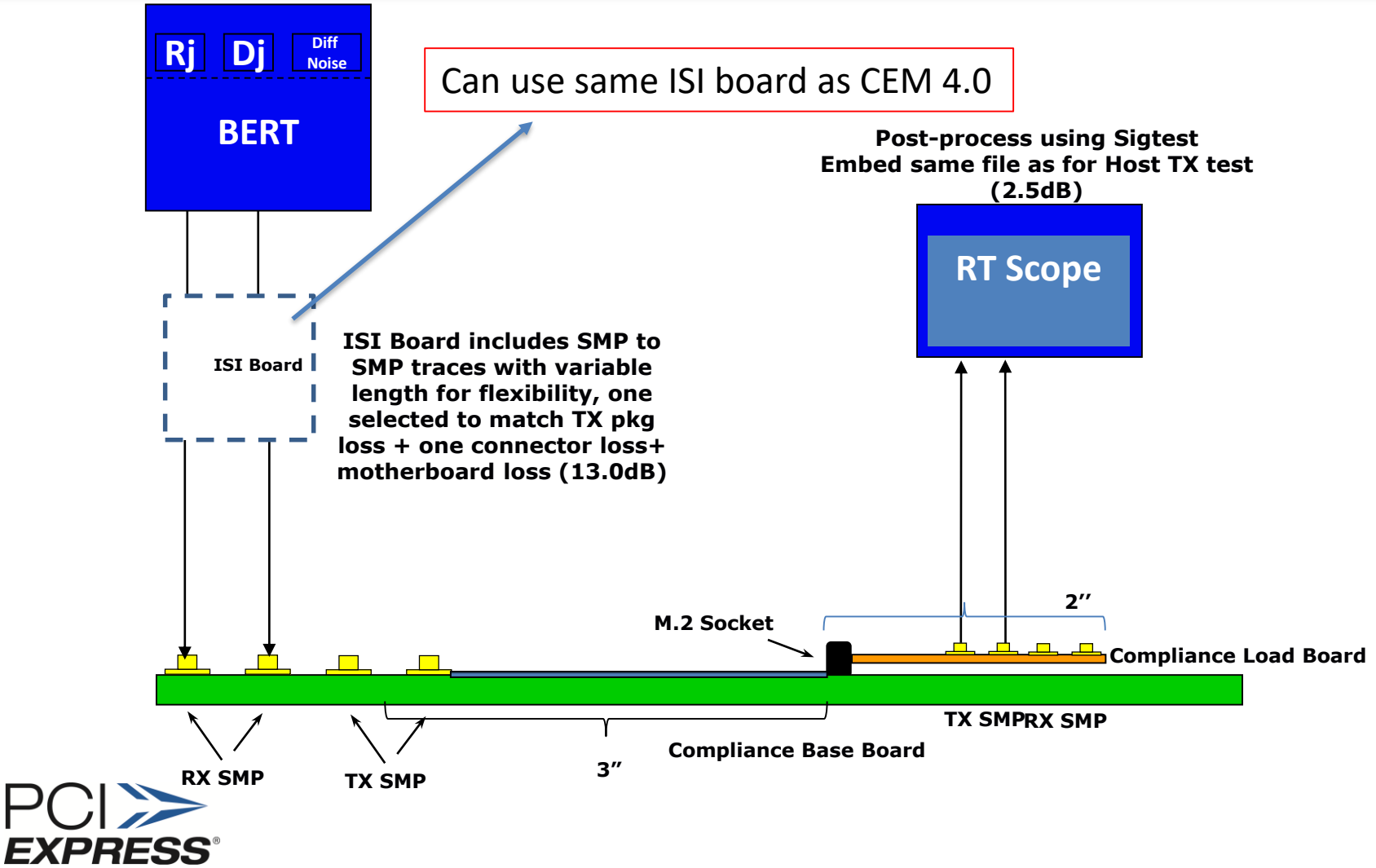
- **Worse case routing on M.2 Add-in Card will be 2”.**
- **Total end to end channel loss will be same as CEM 3.0.**
- **CEM 3.0 Compliance eye limits can be used for M.2.**
- **Not correlating with 4” CEM Add-in card channel. CEM 3.0 simulations were done assuming 4” Add-in Card after the connector. Assuming that change in length distribution does not make significant change.**
- **Assuming same TX/RX package as CEM 3.0.**

Add-in Card TX Test

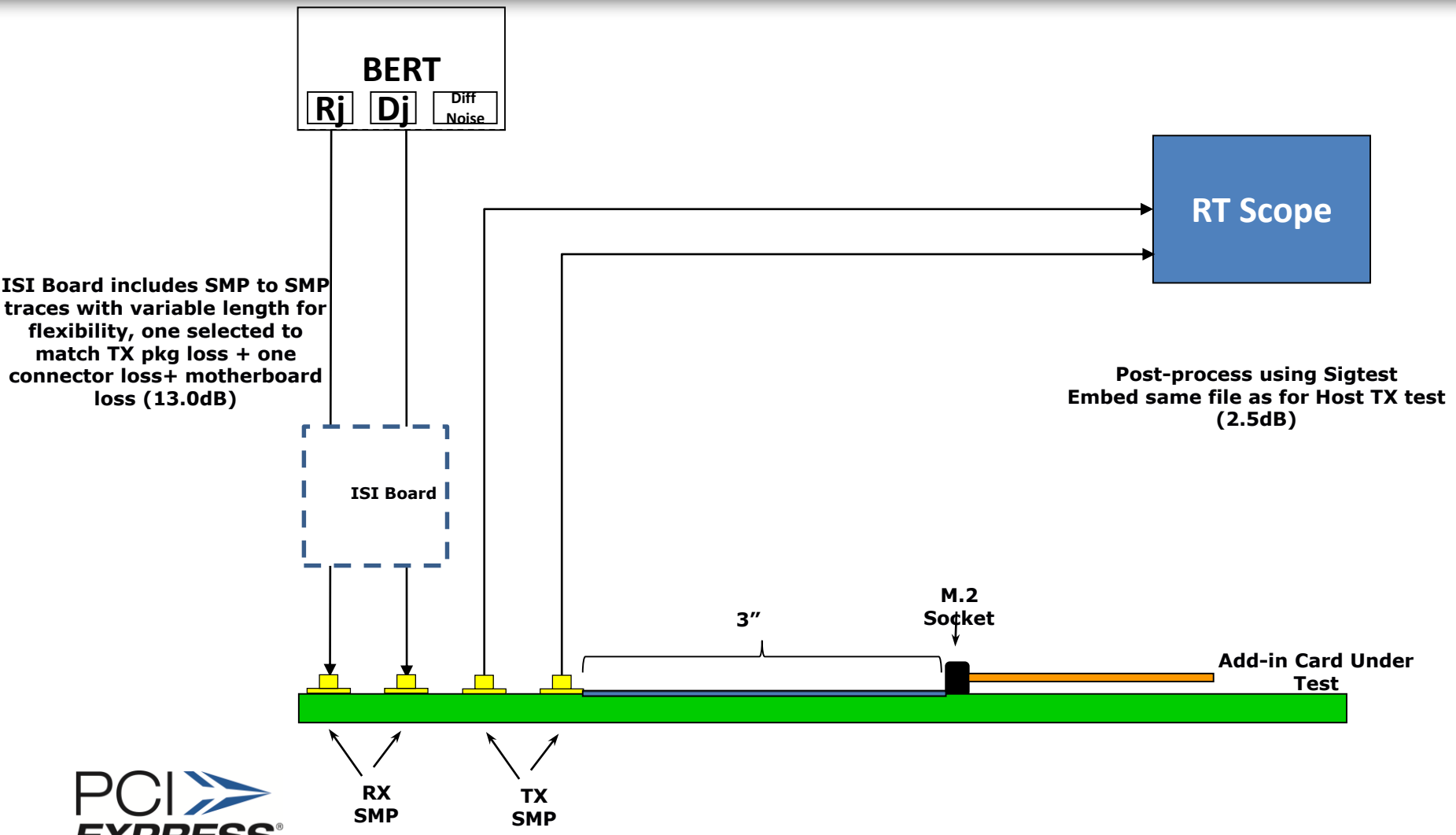


Same as CEM 3.0 limits for Add-in Card TX Test

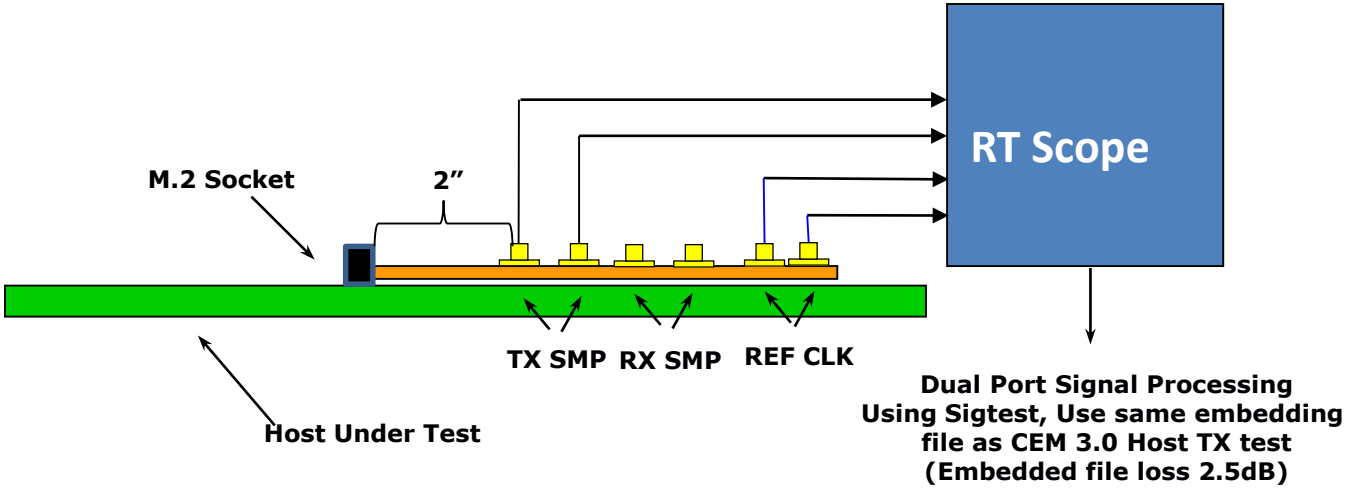
Add-in Card RX Test Calibration



Add-in Card RX Test



Host TX Test



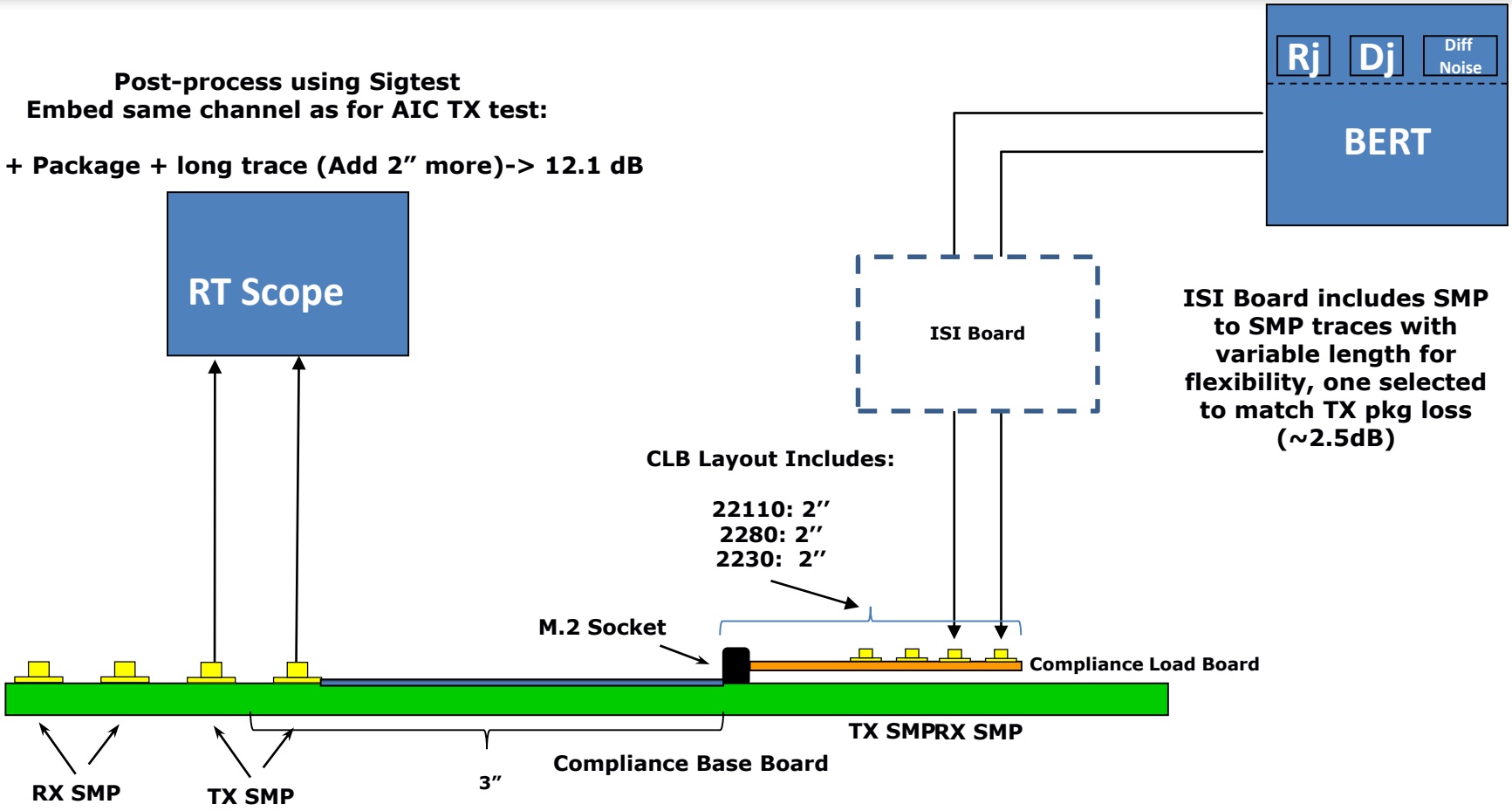
- **Pass: EH > 46mV**
  EW > 41.25ps

Same as CEM 3.0 limits for Host TX Test

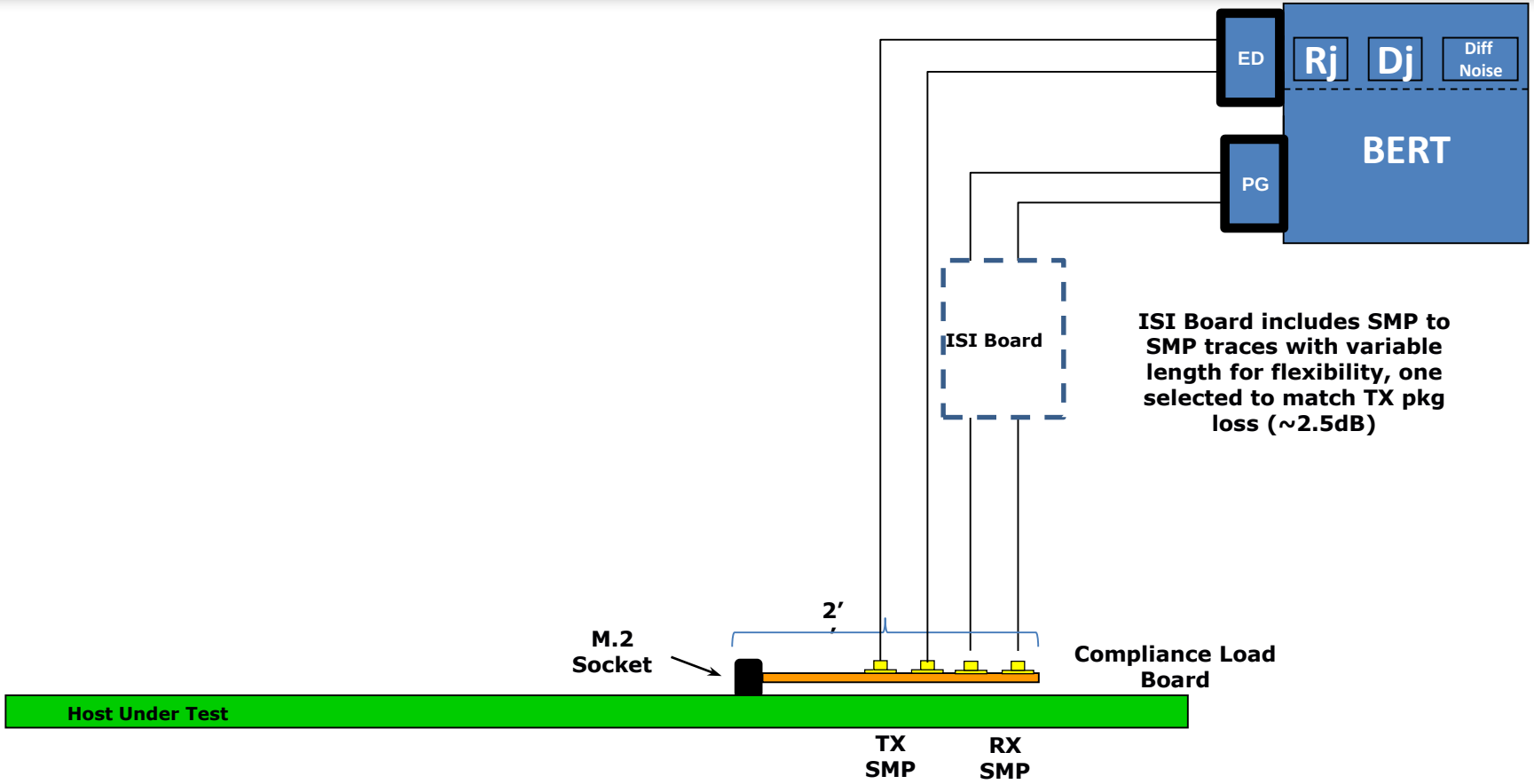
Host RX Test Calibration

Post-process using Sigtest
Embed same channel as for AIC TX test:

Conn + Package + long trace (Add 2" more)-> 12.1 dB



Host RX Test



Review 16GT/s Compliance Proposal for M.2

(Work in progress - subject to change)

16GT/s Compliance Proposal for M.2

- **Possibility of using 8GT/s fixtures for 16GT/s.**
- **CEM 4.0 fixtures- TX and RX break out only.**
  - Additional loss is added using an external ISI board.
- **16GT/s M.2 Add-in Card Insertion Loss being proposed at 6.5dB, for SSDs.**
  - CEM 4.0 budgets 8dB for Add-in Card Insertion Loss.
- **Similar TX and RX test methodology as CEM 4.0 can be adopted for M.2 16GT/s testing.**
- **May need different TX and RX eye limits than CEM 4.0 due to difference in the Insertion Loss budget.**

Timeline

- **M.2 Specification Rev 1.1 was released on Dec 15, 2016.**
- **PCIe Mini WG reviewing M.2 Specification draft Rev 1.2 to be released in Q3’2018 with ECNs and errata discussed in slides above.**

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